a patterned interlevel dielectric material formed on said patterned anti-fuse dielectric layer, wherein said patterned interlevel dielectric includes vias, at least one of said vias has a via space formed above said opening; and

a second level of electrically conductive features formed in said vias and via space(s).

Remarks

The amendment to claim 22 corrects the misspelling and lack of antecedent basis pointed out in the official action. Applicants submit that the amendment does not add any new matter to the disclosure.

Applicants submit that the amendment to claim 22 corrects the informality pointed out in the objection to the claims.

Applicants submit that the terms first and second level of electrically conductive features are adequately defined. The first level of electrically conductive features is discussed at page 9, line 5+ of the present application. A non-limited example of such features is provided in Figure 2 of the present application. Similarly, the formation of electrically conductive features in the vias is discussed at page 13, line 11 wherein the vias are present on a different level from the first level of conductive features. Applicants submit that the invention is not limited to any specific electrically conductive features such that amendment

of the claims to further define these features would be unduly limiting of the invention. Applicants have amended claim 22 to address the antecedent basis for the term spaces. For the above reasons, applicants submit that the claims are now in compliance with 35 USC 112.

The invention centers on novel interconnect structures having an anti-fuse formed as a layer having openings that defines via locations. The structures of the invention advantageously incorporate anti-fuses at reduced manufacturing cost.

Chang (US 5807786) disclose an interconnect structure comprising an amorphous silicon anti-fuse (7) formed over a via hole (3) which hole is defined in dielectric layer (2). In the via hole (3), a further dielectric (6) is located about the top of the via hole as a part of a liner. Chang does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

Go et al. (US 5592016) discloses anti-fuse structures which are located above or below vias. Go et al. does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

McCollum et al. (US 5770885) discloses a silicon oxynitride layer on a substrate over which an amorphous silicon anti-fuse is formed. McCollum et al. does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

For the above reasons, applicants submit that the present claims are patentable over the prior art of record and that the application is in condition for allowance. Such allowance is earnestly and respectfully solicited.

Respectfully submitted,
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Amendments to the Claims

22. (amended) An interconnect structure in which an anti-fuse dielectric is formed therein comprising:

a substrate having a first level of electrically conductive features;

a patterned anti-fuse dielectric layer formed on said substrate, wherein said patterned anti-fuse dielectric layer includes an opening to at least one of said first level of electrically conductive features;

a patterned interlevel dielectric material formed on said patterned anti-fuse dielectric layer, wherein said patterned interlevel dielectric includes vias, [as] at least one of said vias has a via space formed above said opening; and

a second level of electrically conductive features formed in said vias and via [spaces] space(s).